Two flows：

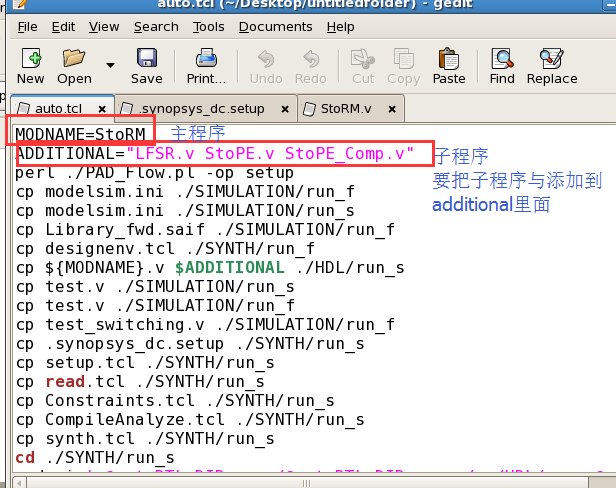
* 图形化（lab2基本操作，lab4 how to write test.v, test\_switching.v）
* Tppe ‘source auto.tcl | tee auto.out’，then excute .vfiles （StoRM.v，test\_switching.v，test.v）（teminal should be opened in the project catalog as the ‘synopsys\_dc.setup’ is in the catalog and it is very important）（toturial,, toturial two describes a whole flow, tells how the command line in ‘auto.tcl’ works ）

In the project files: source auto.tcl | tee auto.out

If you want to run your own design:

First copy the whole folder, change .v files to your own .v files

1. **auto.tcl:**

****

* Modify:

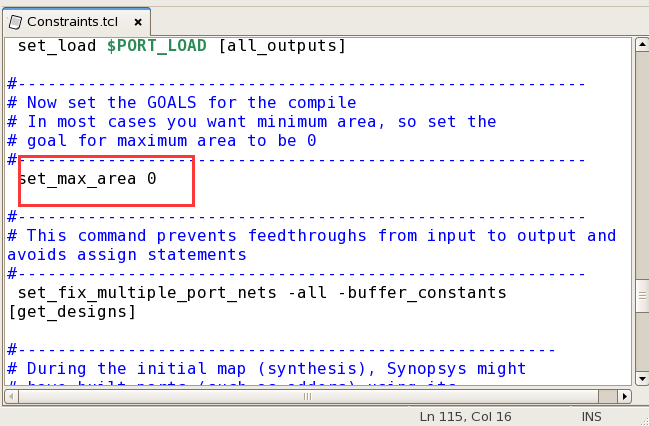
a. modename

b. additional

2. **test.v and test\_switching.v** (power simulation, switching power)

Also can simulate in other software, such as Xilinx ISE.

3. Constraint.tcl (refer to lab 4)



Set goals for the compile.

4. Check result of optimization: synth/run\_f/\*\_final.v

* Move main module to the top (main module is put in the bottom every time the flow executed )
* Load the file in Design Vision to (1)create design schematic;(2)create symbol view;

